Towards Sub-10 nm Diameter III-V Vertical Nanowire Transistors

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Abstract — **Towards the demonstration of sub-10 nm III-V vertical fin and nanowire MOSFETs, a novel alcohol-based digital-etch technology has been developed. The new technique minimizes the mechanical forces exerted on vertical nanowire structures. A consistent 1 nm/cycle etching rate on both InGaAs and InGaSb-based heterostructures has been obtained. This is the first demonstration of digital etch on antimonide-based semiconductors. This technique features a high 97% mechanical yield in the sub-10 nm feature size regime. A record 5 nm diameter InGaAs nanowire with height of 230 nm has been demonstrated. Finally, we fabricated InGaAs vertical single nanowire MOSFETs using this technique. These transistors exhibit a linear subthreshold swing of 70 mV/dec, one of the best values reported in such devices. The results shows promise to demonstrate III-V vertical nanowire transistors with sub-10 nm diameter.**

***Keywords*— Digital etch, InGaAs, InGaSb, nanowire MOSFETs**

I. INTRODUCTION

As CMOS technology keeps advancing, new materials are under active research in the hope of addressing the increasing difficulties of Si in future generations. III-V multi-gate transistors are regarded as some of the most promising candidates. With the physical size of transistors continuing to shrink, it is critical to develop technology to fabricate devices in the sub-10 nm range with high mechanical and electrical reliability. Towards such goal, precise control of the device critical dimensions is a key challenge.

The idea of digital etch (DE), or atomic layer etching, was first developed in silicon [1, 2], and has been adopted to III-V compound semiconductors. In the last few years, the introduction of digital etch has enabled demonstration of aggressively scaled III-V planar and 3D MOSFETs, with impressive electrical characteristics [3-7]. Essentially, during DE, one separates the oxidation and oxide removal steps in a typical semiconductor etching process. Both steps are supposed to be self-limiting in order to afford nanometer-scale control of the etching process. This not only enables precise device dimension engineering, but also mitigates surface damage effectively, such as reactive ion etching (RIE) damage [8].

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Despite the apparent merits of digital etch, the current approach still has two significant drawbacks. First, DE has been only applicable to arsenide-based III-Vs. It does not work on the antimonide-based material system, which is an important class of compound semiconductors with potential for p-channel MOSFETs and tunnel FETs [6, 9-12]. This is because the highly reactive nature of the antimonides easily results in damage during a typical DE process.

Second, though DE has been successful in the arsenides, with demonstrations of 5 nm wide fins [13] and 7 nm diameter lateral nanowires [4]. It is much more problematic in vertical nanowires (VNW). This is because unlike the lateral fins and NWs, there is only one anchoring point. The thinnest VNWs fabricated by DE have been limited to 11-15 nm diameter [6]. The main cause of NW breakage is the strong mechanical stress exerted by the water-based acids used in the oxide removal steps, in addition to the water-based rinsing and drying procedures.

Towards the target of sub-10 nm vertical VNW devices, we have developed a novel alcohol-based DE technique that overcomes these issues. The new approach uses acids dissolved in alcohol in the oxide removal step. We obtain a consistent 1 nm/cycle etching rate on both InGaAs and InGaSb-based heterostructures. We obtain a high mechanical yield of 97% of sub-10 nm VNWs after aggressive DE of 7 cycles. The role of surface tension and viscosity of the etchant solution has been studied. Finally, we demonstrate InGaAs vertical single NW-MOSFETs fabricated by this technique with excellent subthreshold characteristics. We here present an expanded version of an earlier publication [14].

II. ALCOHOL-BASED DIGITAL ETCH

Each cycle of DE of III-V semiconductor consists of an oxidation step, followed by a separate oxide removal step. Oxidation is typically performed either dry in oxygen plasma, or wet in ozonated water or hydrogen peroxide. Oxide removal is mostly performed wet in either sulfuric acid or chloric acid. Both parts should be self-limiting to ensure a controllable etch rate in the nanometer per cycle range.

As explained in the introduction, to deal with the issues of current DE, we explore the use of alcohol-based acids for the oxide removal sub-cycle. The motivation is twofold. On the one hand, we seek to reduce the surface tension and viscosity of the acid removal and rinsing step in an effort to enhance the survivability of very narrow vertical nanowires. Secondly,

we seek a DE technique for antimonides which are highly reactive and easily oxidized and damaged in water. This is particularly the case if there are defects from material growth, a common occurrence since antimonide epitaxial heterostructures are generally not grown lattice-matched to the substrate.

We compare three oxide removal chemistries: 3.0 M HCl in DI water, 2.0 M H_2SO_4 in methanol, and 0.1 M HCl in isopropanol (IPA). All solutions are commercially available. H_2SO_4 and HCl are the most used acids for InGaAs DE. For antimonides, only HCl-based DE is applicable because H_2SO_4 etches antimonides. In all cases, oxidation is performed in oxygen plasma for 3 min in a barrel asher.

The starting arsenide heterostructure consists of multiple layers of $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ grown by MBE on an InP substrate. The antimonide heterostructure consists of 20 nm of $In_{0.28}Ga_{0.62}Sb$ on 200 nm $Al_{0.65}Ga_{0.35}Sb$ buffer, grown by MBE on a GaAs substrate. After standard surface cleaning and native oxide removal, a 2 nm Si_3N_4 adhesion layer is deposited, followed by 100 nm hydrogen silsesquioxane (HSQ), exposed by e-beam to pattern fins and nanowires. The samples are then dry etched by $BCl_3/Ar/SiCl_4$ ICP at 250°C for 2 min, resulting in a final fin or VNW height of about 230 nm for InGaAs and 180 nm for InGaSb.

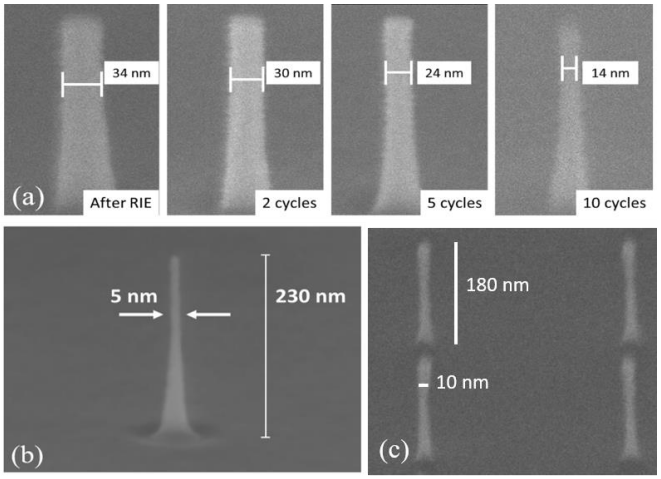

Fig. 1 (a) Evolution of InGaAs VNWs in sequential digital etch in 0.1 M HCl:IPA. (b) InGaAs VNW with 5 nm diameter, 230 nm height obtained after 10 cycles of digital etch in H_2SO_4:methanol. (c) InGaSb VNW with 10 nm diameter, 180 nm height.

After RIE, the arsenide sample is dipped in BOE for 30 s to remove the HSQ mask and native oxide. The antimonide sample is dipped in the HCl:IPA solution for 30 s, to remove the native oxide, with the HSQ remaining. At this point, digital etch cycles are carried out sequentially. Between cycles, fin width and VNW diameter are measured by SEM to monitor the etch rate. Fig. 1(a) demonstrates the digital thinning process of an arsenide VNW with initial diameter of 34 nm, after 2, 5, and 10 DE cycles in HCl:IPA. Fig. 1(b) shows the narrowest arsenide VNW obtained with a 5 nm diameter at the top, where the device layers will be located, and 230 nm height (aspect ratio = 46). Fig. 1(c) shows an antimonide VNW with a 10 nm diameter and 180 nm height. This is the first successful demonstration of DE on antimonides.

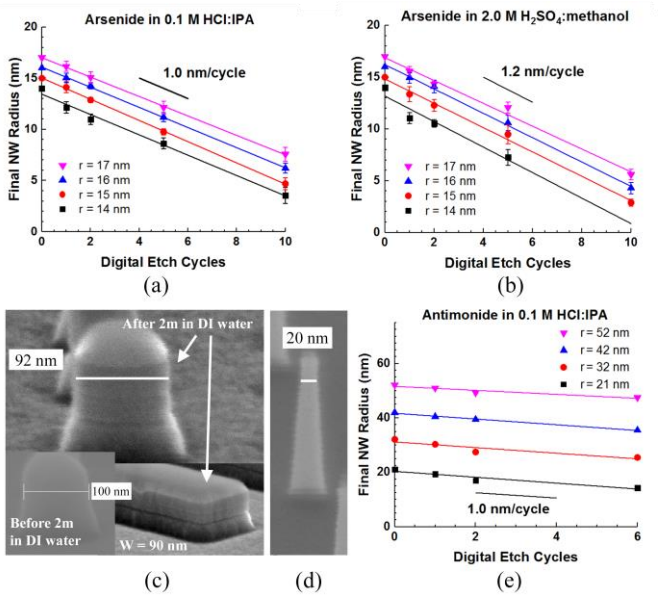

Fig. 2 Etch rate of arsenide VNW radius in (a) 0.1 M HCl:IPA; (b) 2 M H_2SO_4:methanol; (c) Antimonide vertical structures before and after 2 min dipping in DI water; (d) Antimonide VNW after 2 min in HCl:IPA; (e) Same as (a) but for antimonide VNW in 10% HCl:IPA. In (a), (b) and (e), the legends indicate the initial VNW radius before DE.

III. RESULTS AND DISCUSSION

Etch rates were measured from VNW radius on sets of 12 NWs of different initial radius. Figs. 2(a) and (b) show the evolution of arsenide VNW radius in alcohol-based HCl and H_2SO_4, respectively. The average radial etch rate in HCl:IPA is 1.0 ± 0.04 nm/cycle, and in H_2SO_4:methanol is 1.2 ± 0.05 nm/cycle. These values closely match the etch rate using HCl:DI water which is 1.0 ± 0.1 nm/cycle. The cause of slightly higher etch rate in H_2SO_4:methanol is under investigation.

The etching and surface treatment of antimonides is more difficult and less understood. Fig. 2(c) shows the changes of antimonide vertical test structures after dipping in DI water for 2 minutes. Firstly, the diameter decreases from 100 nm to 92 nm. Also, the sidewall and AlGaSb field surface become rough and trenches appear at the heterojunction interfaces. Therefore, water-based DE is not viable for antimonides. Using alcohol-based solutions avoids the undesired etching. Fig. 2(d) shows an antimonide VNW after dipping in HCl:IPA for 2 minutes. No apparent sidewall etching or surface damage can be observed. This indicates that the

HCl:IPA etching is self-limited after it removes the surface oxide on the sidewall. Fig. 2(e) shows the HCl:IPA digital etch rate of antimonide NWs, exhibiting a radial etching rate of 1.0 ± 0.1 nm/cycle.

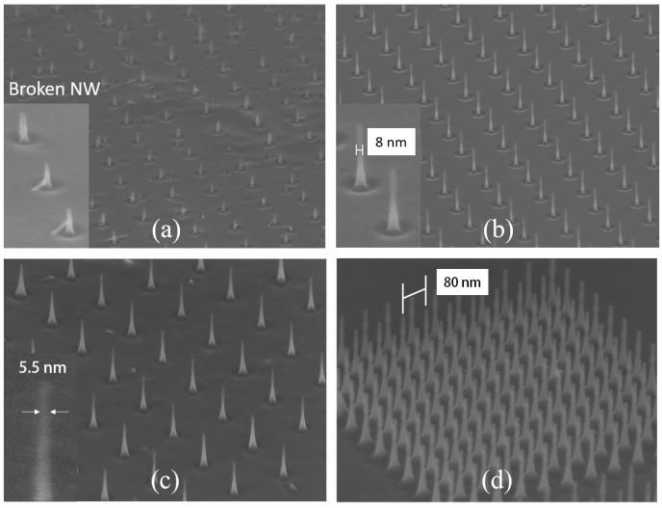

Fig. 3 InGaAs VNW array after 7 DE cycles in (a) 3.0 M HCl in DI water, (b) 0.1 M HCl in IPA, and (c) 2.0 M H_2SO_4 in methanol. The insets show close ups of the VNWs. The NW mechanical yield in (a) is 0%, while the one in (b) is 97% and in (c) is 90%. (d) Tightly-packed arsenide 10 nm VNW array after 7 DE cycles in 0.1 M HCl:IPA.

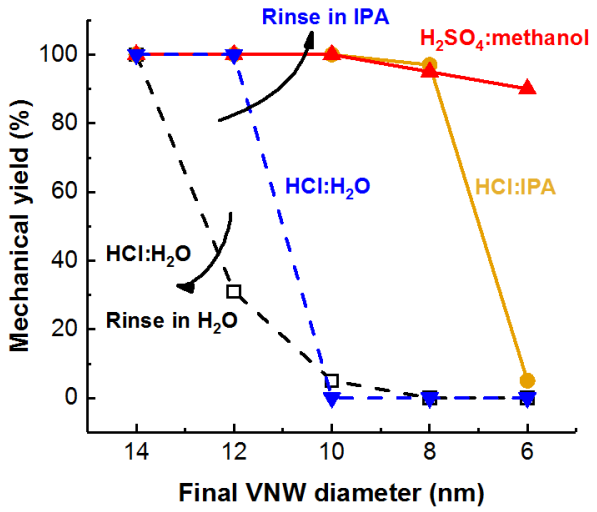

Fig. 4 Mechanical yield of InGaAs VNWs after 7 cycles of digital etch in various etchants and rinsing solutions.

A key challenge for VNW devices fabricated by DE is the poor mechanical yield once the VNW diameter is below 10 nm. This is a result of the high surface tension of water (72 mN/m) during dipping and rinsing, and is problematic for VNWs which, unlike fins, cannot be anchored at both ends. Fig. 3(a) shows an arsenide VNW array (initial diameter = 22 nm) after 7 cycles of conventional DE. A final NW diameter of 8 nm is expected but none survived. In contrast, Fig. 3(b) shows an identical sample processed side-by-side in HCl:IPA, and rinsed in IPA (surface tension = 23 mN/m), and 8 nm diameter VNWs are demonstrated with over 97% mechanical yield. Narrower VNWs below 6 nm can be obtained with over 90% mechanical yield using H_2SO_4:methanol, as shown in Fig. 3(c). Moreover, tightly packed 10 nm VNWs experience no clustering as shown in Fig. 3(d).

We have sought to clarify when VNW breakage occurs. Fig. 4 summarizes the mechanical yield of InGaAs VNWs after 7 DE cycles with various nominal final diameters, for water as well as alcohol-based acids, rinsing in either water or IPA. Fig. 4 clearly demonstrates the superiority of the alcohol-based DE. Starting from left to right, changing the rinse from water (black dashed line) to IPA (blue dashed line) alone improves the yield of HCl:H_2O DE. However, the improvement disappears at D = 10 nm. This suggests that some degree of breakage takes place during the rinsing phase for VNWs of around 12 nm in diameter. Second, changing from HCl:H_2O to HCl:IPA for the oxide removal phase and then rinsing in IPA (yellow continuous line) consistently gives better results all the way down to about 8 nm in diameter. This suggests that a great deal of NW breakage takes place during the oxide etching process itself. Third, changing from HCl:IPA to H_2SO_4:methanol for the oxide removal phase (red line) yields much better results at the smallest diameter of 6 nm. This is likely due to the smaller viscosity of methanol (0.54 cP) when compared with IPA (2.0 cP). All together, these results indicate that VNW breakage happens during both the oxide etch process and while rinsing and that alcohol-based processes are significantly more benign that using water.

It is worth noting that, although there are other drying techniques which can reduce surface tension, such as critical point drying (CDP), solvent-based treatment is most compatible with CMOS manufacturing. Drying methods like CPD are often time consuming, making them impractical when multiple cycles of DE are required. Also, as discussed above, CDP might not be beneficial at/below 10 nm, since the oxide etching process is also responsible for the VNW breakage.

IV. INGAAS VNW-MOSFETs

To illustrate the practical applicability of the new DE process, we fabricate InGaAs VNW-MOSFETs through a process similar to that of [15] using a similar heterostructure to [16]. The process includes 5 DE cycles in 4.1 M H_2SO_4:methanol. Fig. 5(a) shows the schematic cross-section of the device which features a 2 nm thick Al_2O_3 gate dielectric (EOT = 1 nm), W gate metal, and Mo ohmic contacts. NW diameters range from 20 to 40 nm, the channel length is 80 nm.

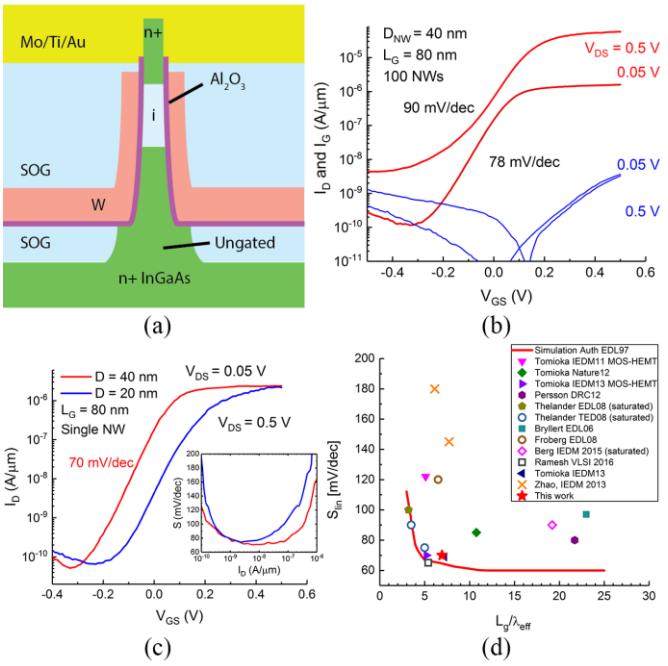

Fig. 5 (a) Schematic cross-section of InGaAs VNW-MOSFET; (b) subthreshold characteristics for a VNW transistor array with D = 40 nm and 100 VNWs, treated with 5 DE cycles in H2SO4:methanol; (c) subthreshold characteristics of a single VNW transistor with D = 40 nm with lowest Slin of 70 mV/dec. The inset shows S vs. ID of this device. (d) Linear subthreshold swing vs. ratio of gate length to natural length of InGaAs VNW MOSFETs.

The linear subthreshold characteristics of a device consisting of 100 NWs with 40 nm diameter is shown in Fig. 5(b). A linear subthreshold swing, S_{lin}, of 78 mV/dec is obtained. Fig. 5(c) shows a single NW device with 40 nm diameter, exhibiting a minimum S_{lin} of 70 mV/dec. The 20 nm diameter device shows a minimum S of 74 mV/dec at V_{DS} = 0.5 V. The D_{it} estimated from the linear subthreshold characteristics is approximately $3.9 \cdot 10^{12}$ $eV^{-1}cm^{-2}$. Devices with narrower diameters suffer from high contact resistance at low V_{DS} due to small top contact area. The inset of Fig. 5(c) shows that S remains below 80 mV/dec over two orders of magnitude of I_D. This is one of the best linear subthreshold swings reported in InGaAs VNW-MOSFETs, as benchmarked in Fig. 5(d), updated from [17]. This indicates that the alcohol-based DE technique delivers sidewall quality comparable to the conventional approach.

V. CONCLUSIONS

In this work, a novel digital etch scheme using alcohol-based etchants for use in III-V nanostructures is reported. The new approach exhibits excellent mechanical yield at sub-10 nm critical dimensions. Digital etch on the antimonide material system is demonstrated for the first time. Vertical nanowire InGaAs MOSFETs have been fabricated using the new technique. Subthreshold characteristics with minimum S of 70 mV/dec and 74 mV/dec are obtained on single NW MOSFET with diameters of 40 and 20 nm, respectively.

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REFERENCES

[1] K. J. Kanarik et al., *JVST. A*, vol. 33, no. 2, pp. 020802.1-020802.15, 2015.
[2] J. Yamamoto et al., *Thin Solid Films*, vol. 225, no. 1, pp. 124–129, 1993.
[3] G. C. DeSalvo et al., *J. Electrochem. Soc.*, vol. 143, no. 11, pp. 3652–3656, 1996.
[4] X. Zhou et al., *VLSI*, 2016.
[5] A. Vardi and J. A. del Alamo, *EDL*, vol. 37, no. 9, pp. 1104-1107, 2016.
[6] E. Memišević et al., *EDL*, vol. 37, no. 5, pp. 549–552, 2016.
[7] N. Waldron et al., *IEDM* 2015, p. 31.1.1-31.1.4.
[8] X. Zhao and J. A. del Alamo, *EDL*, vol. 35, no. 5, pp. 521–523, 2014.
[9] A. Nainani et al., IEDM 2010, pp. 6.4.1-6.4.4.
[10] W. Lu et al., *IEDM* 2015, pp. 31.6.1-31.6.4.
[11] Q. Smets et al., TED, vol. 63, no. 11, pp. 4248–4254, 2016.
[12] W. Lu et al., *CSW* 2017.
[13] A. Vardi et al., *IEDM* 2015, pp. 31.3-1-31-3.4.
[14] W. Lu et al., *EDL*, vol. 38, no. 5, pp. 548-551, 2017.
[15] X. Zhao, A. Vardi, and J. A. del Alamo, *IEDM* 2014, pp. 25.5.1-25.5.4.
[16] X. Zhao et al., *IEDM 2013*, pp. 28.4.1-28.4.4.
[17] J. A. del Alamo et al., *JEDS*, vol. 4, no. 5, pp. 205-214, 2016.